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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 437,579	Applicant(s) MacInnis et al
	Examiner K. Tung	Group Art Unit 2671

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _____3_____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication .
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

☐ Responsive to communication(s) filed on _____1-3-01_____ .

☑ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle,* 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

☑ Claim(s) _____1-2, 4-6 1_____ is/are pending in the application.

    Of the above claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☑ Claim(s) _____1-2, 4-6 1_____ is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claim(s) _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 11 9(a)-(d).

    ☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been
    ☐ received.

    ☐ received in Application No. (Series Code/Serial Number)_____ .

    ☐ received in this national stage application from the International Bureau (PCT Rule 1 7.2(a)).

    *Certified copies not received:_____ .

Attachment(s)

☑ Information Disclosure Statement(s), PTO-1449, Paper No(s). 7, 9   ☐ Interview Summary, PTO-413

☐ Notice of Reference(s) Cited, PTO-892   ☐ Notice of Informal Patent Application, PTO-152

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948   ☐ Other_____

Office Action Summary

DETAILED ACTION

1.   The amendment filed 1/3/01 has been considered in preparing this office action.

Claim Rejections - 35 USC § 112

2.   Claim 2 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for

failing to particularly point out and distinctly claim the subject matter which applicant regards

as the invention.

As per claim 2, "the memory" is indefinite since it is unclear which memory is being referred

to, the local memory or the external memory.

3.   Claims 1-2, 4-29 and 61 are rejected under 35 U.S.C. 112, first paragraph, as

containing subject matter which was not described in the specification in such a way as to

reasonably convey to one skilled in the relevant art that the inventor(s), at the time the

application was filed, had possession of the claimed invention.

The feature "a graphics accelerator comprising a processor and a coprocessor" in claim 1 is

not described nor illustrated in the drawings.

The feature "transferring a third block of processed graphics data from the on-board memory

to the main memory while the first block of graphics data is being processed" in claim 61 is also not

described nor illustrated in the drawings.

Claim Rejections - 35 USC § 103

4.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section
102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the
subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary
skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the
invention was made.

5.   Claims 1-2, 4-5, 19, 23-29-31, 37, 44, and 50-58 are rejected under 35 U.S.C. 103(a)

as being unpatentable over Ben-Yoseph et al (5,949,439) in view of Gulick et al (5,758,177).

Ben-Yoseph et al teaches a graphics accelerator (Fig. 1) comprising a processor (106) for

processing graphics data; a local memory (SRAM 146) for storing graphics data, the graphics data

including pixels; a coprocessor (106) for performing operations on a plurality of components of one

pixel of the graphics data (col. 3, lines 11-39); and a DMA engine (inherent by the teachings of DMA

operations of Ben-Yoseph et al, col. 4, lines 36-40 and col. 4, line 62 to col. 5, line 4). It is noted

that Ben-Yoseph et al fails to explicitly suggest the multimedia processor (106) comprising two

separate processors. Ben-Yoseph et al teaches the multimedia processor 106 is a single, multiple

function, multimedia processor that performs multiple functions that have conventionally been

performed using separate fixed function accelerators for graphics and audio functions (col. 3, line 66

to col. 4, line 7). Thus, the teachings of two separate processors would have been obvious by Ben-

Yoseph et al at the time of invention. Furthermore, Gulick et al teaches a multimedia processor (Fig.

2) comprising a video/graphics engine (202), general purpose DSP (206), DMA engine (236),

memory buffer (234), an audio engine (204) ... It would have been obvious to one of ordinary skill

in the art at the time the present invention was made to combine the teachings of Gulick et al into the system of Ben-Yoseph et al in order to incorporate separate processors into same chip and thus to reduce the size and add speed without lost the flexibility. Therefore, at least claims 1 and 2 would have been obvious by Ben-Yoseph et al and Gulick et al.

As per claims 4 and 5, Ben-Yoseph et al teaches the coprocessor processes the plurality of components of each pixel, RGB components, in parallel as three elements of a vector (inherent by any 3D graphics pixel data which normally in RGB format and YUV for video data).

As per claim 19, Ben-Yoseph et al teaches the coprocessor has an instruction set that includes a special instruction for comparing between each element of a pair of 3-element vectors (inherent by the VLIW, col. 3, lines 35-39).

As per claim 23, Ben-Yoseph et al teaches the DMA engine moves data between the memory and an external memory at the same time the graphics accelerator is using the memory for its load and store operations (col. 4, lines 36-40 and col. 4, line 65 through col. 5, line 4 and Gulick et al, col. 6, lines 42-46).

As per claim 24, Gulick et al suggests the external memory is a unified memory that is shared by a graphics display system, a CPU and other peripheral devices (col. 6, lines 39-46 and Fig. 7, 110 and Gulick et al obvious by the memory buffer 234).

As per claim 25, Ben-Yoseph et al teaches the DMA engine includes a queue to hold a plurality of DMA commands (inherent by portion of SRAM 146, col. 5, lines 50-62 and/or software queue 144).

As per claim 26, Ben-Yoseph et al teaches the plurality of DMA commands are executed in the order they are received (inherent by any FIFO buffer and/or software queue 144 and Gulick et al, also would have been obvious by the memory buffer 234 in FIFO type).

As per claim 27, Ben-Yoseph et al teaches the queue comprises a mechanism that allows the graphics accelerator to determine when all the DMA commands have been completed (read and write pointers 136 and 138, col. 5, lines 26-30 and Gulick et al, would be obvious by any read and write pointers).

As per claim 28, Gulick et al teaches the queue is four deep for storing up to four DMA commands (would be obvious by any FIFO to configure into any reasonable size (storage capacity)).

As per claim 29, Ben-Yoseph et al teaches the graphics accelerator is working on operands and producing outputs for one set of pixels, while the DMA engine is bringing in operands for a future set of pixel operations (inherent by the teachings of FIFO type queue or portions of SRAM of Ben-Yoseph et al and/or software queue 144 and Gulick et al, inherent by the teachings of buffer 234 because this is what the buffer for).

Claim 30 is similar in scope to claim 1, and additionally requires concurrently transferring blocks of unprocessed data and processed data between the main memory and the local memory while the block of graphics data is being processed (would have been obvious by the teachings of Ben-Yoseph et al, col. 3, lines 40-65).

The method claim 31 is similar in scope to the apparatus claim 5, and thus is rejected under similar rationale.

As per claim 37, Ben-Yoseph et al teaches each of the plurality of pixels of graphics data comprises YUV components of YUV formatted graphics data (col. 5, lines 5-7).

Claim 44 is similar in scope to claim 19, and thus is rejected under similar rationale.

Claims 50-58 are similar in scope to claims 1 and 23-29, and thus are rejected under similar rationale.

Claim 59 is similar in scope to the combination of claims 25 and 26, and thus is rejected under similar rationale.

As per claim 60, Ben-Yoseph et al teaches the coprocessor incorporates load and store functions for unpacking graphics data into a plurality of components, processing each of the plurality of components, and converting the plurality of components into a format suitable for storage (Fig. 1, col. 4, line 11 through col. 5, line 19).

Claim 61 is similar in scope to claim 30, and additionally requires transferring third block of processed graphics data from the on-board memory to the main memory while the first block of graphics data is being processed (would have been obvious by Ben-Yoseph et al since Ben-Yoseph et al teaches simultaneously transmits and receives data over a high speed Rambus DRAM channel, col. 3, lines 40-56).

6.   Claims 6-18, 20-22, 32-43, and 45-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ben-Yoseph et al (5,949,439) and Gulick et al (5,758,177) as applied to claims 1 and 30 above, and further in view of Hancock (5,604,514).

The teachings of Ben-Yoseph et al and Gulick et al are given in previous paragraph of this office action. However, Ben-Yoseph et al and Gulick et al fails to explicitly mention the pixels are in an RGB16 format. Ben-Yoseph et al teaches receiving video data in an 16-bit YUV format. It was old and well known and well use in the art that the pixel data can be any format, such as, RGB16, RGB8, RGB24, YUV8, YUV16, or YUV24 etc ... Furthermore, Hancock teaches the pixel data RGB16, YUV16, etc ... (Fig. 3, col. 3, line 52 through col. 4, line 6, col. 5, lines 6-17). It would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teachings of Hancock into the system of Ben-Yoseph et al and Gulick et al in order to improve video subsystem fro concurrently displaying graphics and image data as taught by Hancock (col. 2, lines 28-30). Therefore, at least claims 6-8, 13-16, 32-33, 37-40 and 45-46 would have been obvious by Ben-Yoseph et al, Gulick et al and Hancock.

As per claim 9, Ben-Yoseph et al teaches the two pixels are respectively selected by two special load instructions (col. 3, lines 57-65).

As per claim 10, Ben-Yoseph et al teaches the two special load instructions are for loading a left one and a right one of the two pixels, respectively (150 and col. 3, lines 35-65).

As per claim 11, Ben-Yoseph et al teaches the coprocessor comprises an input register (SRAM 146).

As per claim 12, the combined system fails to specifically suggest the RGB components are expanded into 8-bit components through zero expansion when loaded into the input register. How, it would have been obvious to one of ordinary skill in the at the time the present invention was made

to implement the teachings of MPEG decode of Ben-Yoseph et al and Hancock in order to obtain the claimed feature.

As per claims 17 and 18, Ben-Yoseph et al teaches the two pixels are respectively selected by two special load instructions for extracting a first one and a second one of the two pixels, respectively (150 and col. 3, lines 35-65).

As per claim 20, Ben-Yoseph et al teaches a result register for storing the results of the three comparisons (col. 5, lines 50-62).

As per claim 21, the combined system fails to explicitly teach the results of the three comparisons are used together during a single conditional branch operation. It would have been obvious to one of ordinary skill in the art at the time the present invention was made to implement the teachings of using VLIW technology and instruction unit of Ben-Yoseph et al in order to increase system processing performance.

As per claim 22, the combined system also fails to explicitly teach the special instruction is for a greater-than-or-equal-to operation. It would have been obvious to one of ordinary skill in the art at the time the present invention was made to implement the teachings of Ben-Yoseph et al in order to compare the operands or data.

Claims 34-36, 41-43 and 47-49 are similar in scope to claims 9, 10, 17, 18, 20, 21, and 22, and thus are rejected under similar rationale.

Response to Arguments

7.   Applicant's arguments filed 1/3/01 have been fully considered but they are not

persuasive.

The rejections have been modified in order to fully considered applicant's amendment.

Conclusion

8.   Applicant's amendment necessitated the new ground(s) of rejection presented in this

Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a).

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS

from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the

mailing date of this final action and the advisory action is not mailed until after the end of the

THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the

date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be

calculated from the mailing date of the advisory action. In no event, however, will the statutory

period for reply expire later than SIX MONTHS from the date of this final action.

Responses

9.   Responses to this action should be mailed to:
          Commissioner of Patents and Trademarks
          Washington, D.C. 20231.

If applicant desires to fax a response, (703) **308-9051(52)** may be used for formal communications or (703) **308-5403** for informal or draft communications.

Please label "PROPOSED" or "DRAFT" for informal facsimile communications. For after final responses, please label "AFTER FINAL" or "EXPEDITED PROCEDURE" on the document.

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).
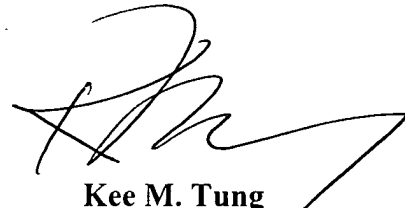
Inquires

10.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Kee M. Tung** whose telephone number is (703) **305-9660**. The examiner can normally be reached on **Tuesday - Friday** from **6:30 am to 5:00 pm**.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Mark Zimmerman**, can be reached on (703) **305-9798**.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) **308-4700**.

Kee M. Tung
Primary Examiner
Art Unit 2671

February 6, 2001